

EXPERIMENT

1

Logic Gate Parameters

VERSION F04

In this experiment, you will become familiar with the terminal characteristics and parameters for digital logic gates viewed as electronic circuits. After performing this experiment, you should be able to use a mixed signal oscilloscope to:

- 1) Display the voltage transfer characteristic of a logic gate,
- 2) Find the operating points of a gate representing the HIGH and LOW logic levels,
- 3) Find the noise margins of a gate,
- 4) Find the propagation delay of a gate,
- 5) Display digital signals on an oscilloscope with logic analyzer-like features, and
- 6) Apply lab skills learned in subsequent experiments.

1-1 PRELAB

IMPORTANT NOTICE: If you have this available before your first lab, please study this prelab material before going to lab. You will still be able to do the lab based a brief presentation by your lab instructor even if you are unable to study ahead. In this case, it is important that you study the prelab material before doing the laboratory report.

This experiment requires a number of concepts, some of which may be new to you. Section 2-8 of Mano and Kime [1] covers the basic terminology. Concepts covered or reviewed here are: 1) voltage transfer characteristics, 2) operating points, 3) noise margins, and 4) propagation delay.

VOLTAGE TRANSFER CHARACTERISTICS

The *static voltage transfer characteristic* of a logic gate is simply a plot of the gate output voltage V_{OUT} versus the gate input voltage V_{IN} . We can mathematically describe the transfer characteristic as $V_{OUT} = f(V_{IN})$. We use the word *static* to describe the transfer characteristic because it represents behavior in response to slowly changing signals so that dynamic effects such as the delaying of the signal from gate input to gate output are avoided in measurements.

Figure 1-1(a) shows an ideal static transfer characteristic for an inverter with input V_{IN} , output V_{OUT} and power supply voltage, $V_{CC} = 5.0$ V. What can we learn from a static transfer characteristic that is useful in characterizing gate operation? In order to answer this question, we need to define some terminology.

First, we will consider the *operating points* for the inverter. These points correspond to the HIGH and LOW values on the outputs of the inverter. Since the output voltage depends on the input voltage, to find the value of the HIGH operating point for an inverter output, the value of the LOW operating point for the same inverter needs to be applied to its input. Likewise, to find the value of the LOW operating point, the value of the HIGH operating point needs to be applied. This requires that we know the values we are trying to determine! By analytically using feedback, we can combine the transfer characteristics of two identical inverters to achieve this dependency relationship.

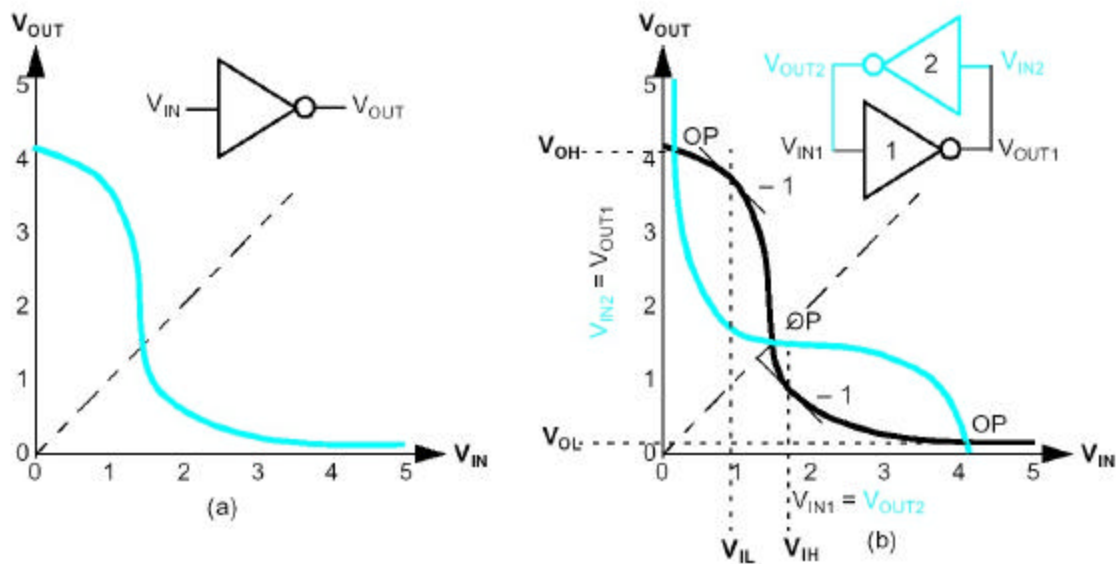


Figure 1-1 Transfer Characteristic and Operating Points

This is done by connecting two inverters in a loop as shown in Figure 1-1(b). For the two inverters, we note that $V_{IN2} = V_{OUT1}$ and $V_{IN1} = V_{OUT2}$. Since both of the inverters have the same transfer characteristic, we take the transfer characteristic of inverter 2 and mirror it about the $V_{OUT} = V_{IN}$ line so that its V_{IN} axis lies coincident with the V_{OUT} axis of the transfer characteristic for inverter 1 as shown in Fig. 1-1(b); then the V_{IN} axis of gate 1 also coincides with the V_{OUT} axis of gate 2. By this mirroring operation, the relationships given in Fig. 1-1(b) are satisfied on the axes of the plot. Because of the voltage equalities, the only points where both static transfer characteristics can be satisfied on this plot is where they intersect. These intersection points are $(V_{IN1} = 0.15 \text{ V}, V_{OUT1} = 4.05 \text{ V})$, $(V_{IN1} = 1.50 \text{ V}, V_{OUT1} = 1.50 \text{ V})$, and $(V_{IN1} = 4.05 \text{ V}, V_{OUT1} = 0.15 \text{ V})$; these operating points are marked with OP. A small change in V_{IN1} from 1.5 V will cause departure from the $(V_{IN1} = 1.5 \text{ V}, V_{OUT1} = 1.5 \text{ V})$ point toward one of the other two points. Thus, this point is *unstable*, will not persist, and is of little interest. Small departures from the other two operating points, however, are reversible and with the appropriate change in V_{IN1} will result in a return to those points. These are *stable operating points* for the inverters. They define the voltage values that correspond to HIGH and LOW on inputs and outputs of this particular inverter. Since we are using *positive logic*, HIGH corresponds to 1 and LOW corresponds to 0. Thus for the given inverter, the voltage values for 0 and 1 are 0.15 V and 4.05 V, respectively. For V_{OUT} , the LOW value is *V output LOW*, denoted V_{OL} , and the HIGH value, *V output HIGH*, denoted V_{OH} .

So, for this inverter, V_{OL} is 0.15 V and V_{OH} is 4.05 V. Finally, since the LOW value on the input produces a HIGH value on the output and vice-versa, an inversion of the voltage values has occurred. For either positive or negative logic, the inverter is also often called a NOT gate since it *negates* the input value to produce the output value. Note that if you actually connected two identical gates in a loop, you would get only an operating point, not the transfer characteristics. In the lab, we will generate the equivalent of Fig. 1-1(b) for two inverter types.

Next, we define the concept of noise margins; our approach is that used in Kang and Leblebici [2]. Noise is assumed to be an effective voltage on one or more inputs to a gate that is added to or subtracted from the voltage normally present. The normal voltage is a stable operating point voltage. Examples of sources of noise are fluctuations in the power supply voltage V_{CC} , noise generated by other digital circuits changing values rapidly, or external electromagnetic radiation. Intuitively, noise margins represent the amount of effective noise voltage that can be tolerated on an input without seriously disturbing the gate output.

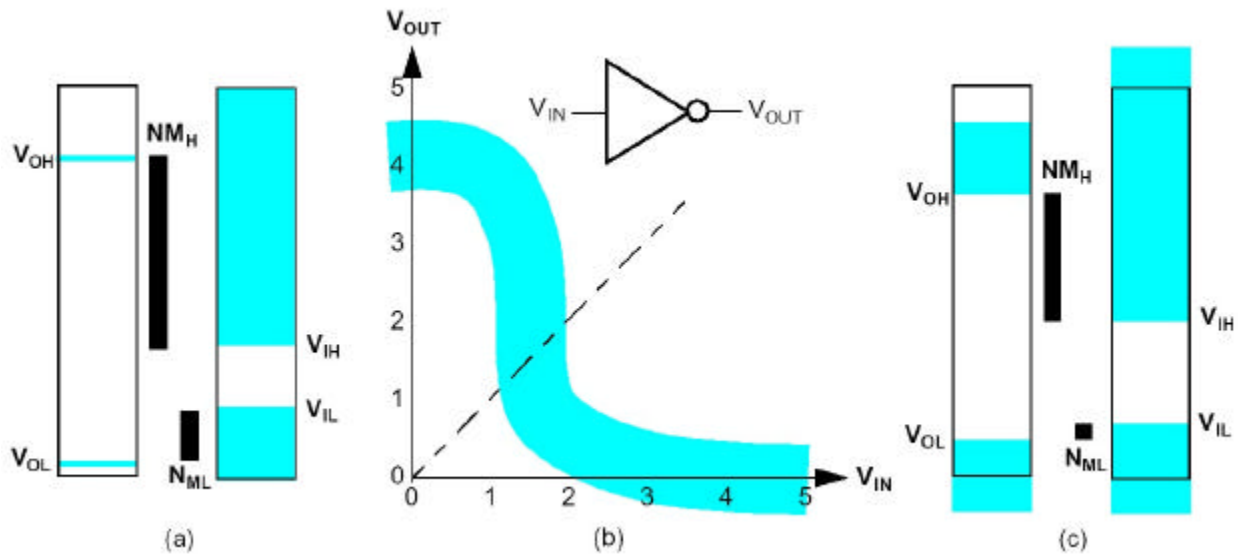


Figure 1-2 Noise Margins and Logic Family Transfer Characteristics

In order to evaluate the noise margins, we need to define two additional voltages from the transfer characteristic. These are the two input voltages at which $dV_{OUT}/dV_{IN} = -1$. The lower of these two voltages is *V input LOW* denoted by V_{IL} , and the higher is *V input HIGH* denoted by V_{IH} . These voltages are chosen somewhat arbitrarily as the *highest* value that will act as a LOW input and the *lowest* value that will act as a HIGH input. Intuitively, this makes some sense in that if any voltage between these two voltages is applied to the input, any noise superimposed on that voltage produces a larger noise voltage on the output, i.e., the noise voltage is amplified. This amplification of noise is interpreted as a serious disturbance of the gate output. For the inverter in Fig. 1-1, $V_{IL} = 0.90$ V and $V_{IH} = 1.70$ V.

With these two values plus V_{OH} and V_{OL} , we can define the *static voltage noise margins* for a logic gate. The *LOW noise margin*, is $NM_L = V_{IL} - V_{OL}$, and the *HIGH noise margin* is $NM_H = V_{OH} - V_{IH}$. *Static* again means that dynamic effects are ignored and implies that the margins may not apply for high frequency noise. For the inverter transfer characteristic in Fig. 1-1, the noise margins are $NM_L = 0.90 - 0.15 = 0.75$ V and $NM_H = 4.05 - 1.70 = 2.35$ V. The intuitive implication of these values is that 1) an input noise voltage of 0.75 V added to input V_{OL} gives an output that would still be interpreted as a HIGH, and 2) an input noise voltage of 2.35 V subtracted from input value V_{OH} gives an output that would still be interpreted as a LOW. We will calculate the noise margins for two inverter types in the lab and compare them.

Now we can consider fully the question: “What is a logic 0 and what is a logic 1 (for positive logic)?” For the inverter just analyzed, a 0 on an output has value 0.15 V and a 1 on an output has a value of 4.05 V. However, on the input, any voltage between GND and 0.90 V is a logic 0 and any voltage between 1.70 V and VCC is a logic 1. This is shown pictorially in Fig. 1-2(a). So we have defined the physical meaning of 0 and 1 in terms of voltages values and ranges.

In general, these physical values are specified for an entire family of gates, for many different production lots, for different loading on the outputs, for variation in the power supply values, and for a broad range of operating temperatures. The results are a large number of transfer characteristics which collectively might appear as in Fig. 1-2(b). From this collection of curves, we find the range of values which appears on the outputs and the range of values that can act as valid inputs by using the same techniques as employed for the individual characteristic in Fig. 1-1 and take the worst case values for each voltage. The end result, as illustrated in Fig. 1-2(c), is the definition of logic 0 and logic 1 for the entire family of

gates. We note that in this case, with all of the variations taken into account, the noise margins become smaller than for the individual gate.

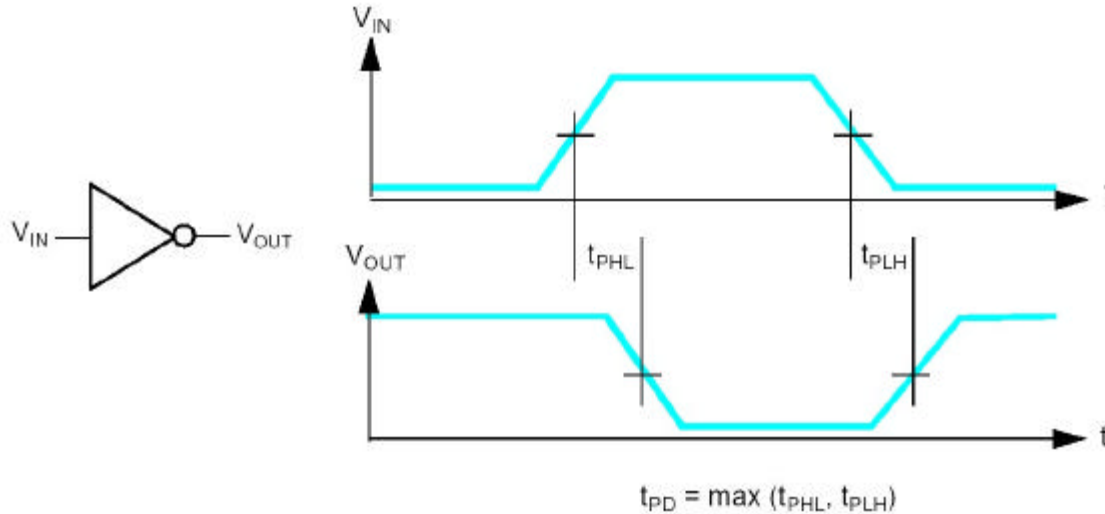


Figure 1-3 Gate Delay Parameter Definitions

GATE DELAY

Here we consider two primary gate delay parameters. In order to define these parameters, we will use an inverter as an example. We will assume that a pulse is applied to the inverter input V_{IN} as shown in Fig. 1-3. The response to this pulse on the output of the inverter is V_{OUT} , also shown in Fig. 1-3. The two parameters are the *high-to-low propagation time*, t_{PHL} and the *low-to-high propagation time*, t_{PLH} . We make both of these timing parameter measurements at the 50% level on the waveforms for V_{IN} and V_{OUT} . Formally, the 50% level is defined as the voltage $0.5(V_{OH} - V_{OL}) + V_{OL}$. t_{PHL} is the time measured from this voltage on the rising input waveform to the same voltage on the falling output waveform. t_{PLH} is the time measured from this voltage on the falling input waveform to the same voltage on the rising output waveform. Note that the subscripts on these parameters refer to the direction of change on the *output* waveform. These two gate delay times are defined graphically on the waveforms in Fig. 1-3. In addition, we define a secondary parameter, the worst case propagation delay, $t_{PD} = \text{Maximum}(t_{PHL}, t_{PLH})$. It should be noted that the 50% level for measuring delay is not universally used. For example, some manufacturers use 1.3V as the level for delay measurement for Low Power Schottky Transistor-Transistor Logic (LSTTL). Also, t_{PD} does not universally represent the maximum propagation delay for a single gate. Some text authors use t_{PD} to represent the average of t_{PHL} and t_{PLH} ; we will call this $t_{PD(\text{average})}$. Returning to t_{PD} for the case of many inverters of the same type, we are taking the worst case (maximum) values that can possibly occur for each of t_{PHL} and t_{PLH} and then taking the maximum of these two values. The end result, t_{PD} , is the longest delay that can ever occur for a signal change propagating from an input of a gate to the output of the gate, regardless of the direction of the signal changes. These same parameters can also be defined from a given input to a given output of more complex integrated circuits or parts thereof.

PRELAB WRITEUP

There is no prelab write-up for this lab, but you are expected to thoroughly study the prelab material before or after the lab.

1-2 LAB WORK

ON REPORTS: All lab results and all answers to questions or discussion are to appear in the lab reports of individual students. All tangible lab results are to be identical; when a printout of results is specified, a copy should be made for each team member. All answers to questions or discussion are to be the work of individual students, **not** the lab team. Evidence of collaboration on these aspects of a report within or between teams will be noted and is subject to University disciplinary action.

In this experiment, you will find the voltage transfer characteristics and parameters for two device in the High-speed Complementary Metal Oxide Semiconductor (HCMOS) logic family. In addition, you will verify the function of an HCMOS 3-input NOR gate.

EQUIPMENT NEEDED

In addition to the equipment already on the lab bench, your instructor will have you check out a plastic tray containing:

- 1) an ECE351 logic board.
- 2) a power supply module for the logic board,
- 3) two scope probes,
- 4) a logic analyzer probe,
- 5) four black logic analyzer extension lead in a plastic bag,
- 6) a coaxial cable with BNC connectors.

WARNING – LAB EQUIPMENT HANDLING: Much of the lab equipment is small and delicate. In particular, this applies to the FPGA boards, scopes, scope probes, and logic analyzer probes. So please be careful and handle the equipment with a light and careful touch and do not use the scope probes with the grabbers removed. Perform wiring on the board **ONLY** with the power and other cables disconnected!

INITIAL SETUP

- 1) Verify that the Wavetek signal generator power is off. (The power switch for the Wavetek is located on the back.)
- 2) Place the logic board and its power supply in front of signal generator and scope, but do not connect the power to the logic board as yet.
- 3) Connect MAIN OUT on the Wavetek to the BNC connector on the left side of the logic board carrier by using the coaxial cable.
- 4) Carefully attach the two scope probes and the logic analyzer probe to the scope. The logic analyzer probe needs to be well seated, but there is no sound or locking action, so don't push it in too hard. Note the colored rings on the necks of the probes near the connectors to the scope; the same colored rings appear at the grabber end of the probes so you can easily identify the probe grabber corresponding to each of the channels.
- 5) Turn on the oscilloscope power.

74HC04 VOLTAGE TRANSFER CHARACTERISTIC AND NOISE MARGINS

Objective: To find the transfer characteristics and static noise margins for a 74HC04 CMOS inverter.

SETUP

- 1) Look at the logic board. Note the headers numbered JP1 through JP5 along the front of the board. These jumpers are connected to the three small scale integrated (SSI) circuits (IC1-3) along the center of the board. These are the circuits that we will be using in this experiment. Also, note the BNC connector J1 at the left edge of the board. This connector will be used to supply a signal from the Wavetek generator to the circuits. The pin header labeled GROUND will be used to attach the ground connections of the scope probes. The remaining pin headers (JP1-JP5) are used to make connection to the SSI devices.

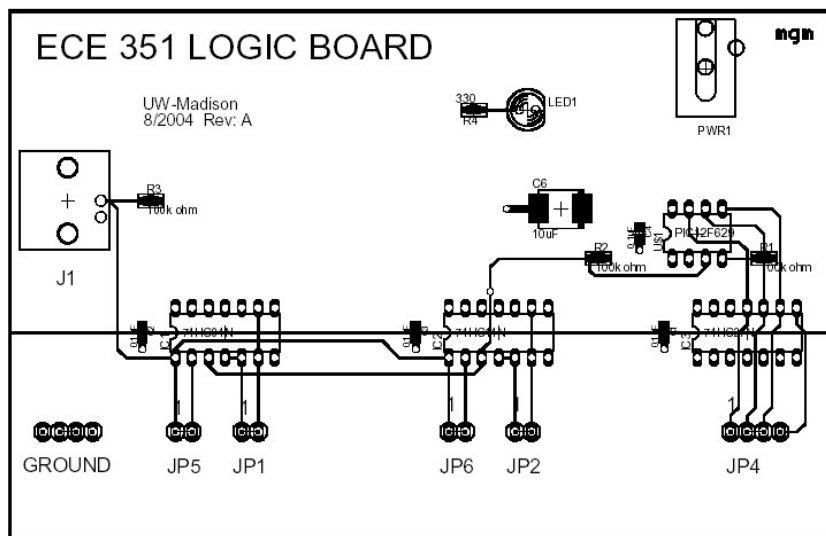


Figure 1-4 Logic Board Locations

- 2) Ensure that the Wavetek generator is OFF, then connect the Wavetek generator MAIN OUT to the BNC connector J1 using a short BNC-BNC cable. This connects the generator to pin 1 of the 74HC04 IC (integrated circuit) as shown below in Figure 1-4.
- 3) Locate pin 1 of JP5, which is connected to the input of the first inverter, of the 74HC04.

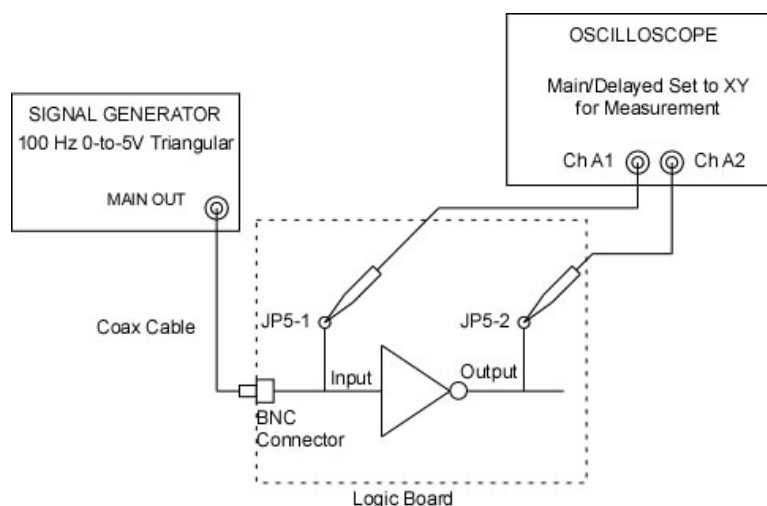


Figure 1-5 Setup for Finding Transfer Characteristics

- 4) Take two of the black logic analyzer extension leads from the plastic bag. Connect it to JP5-1 (this connects to pin 1 on the 74HC04) and grab the pin on this lead with the “grabber” (NOT the ground clip) on the scope probe attached to channel A1.
- 5) Connect a second black lead to JP5-2 (connects to pin 2 on the 74HC04) and grab with the scope probe connected to channel A2
- 6) Connect both scope probe ground clips to the 4-pin connector labeled GROUND at the left edge of the logic board. This completes the physical setup in Fig. 1-5 for making the transfer characteristic measurement.

WARNING – GND CONNECTIONS: Be very careful not to connect a ground clip or ground lead from the oscilloscope to VCC instead of GND! This can result in a short that causes the lead to get hot or to melt!

- 7) On the Wavetek generator, set DC OFFSET to 0 (center position) and set AMPLITUDE to minimum (fully counterclockwise).
- 8) Connect the circular power plug to the right rear of the FPGA board and plug the power supply into the outlet.
- 9) Turn the Wavetek power ON.
- 10) On the Wavetek, push the Display Select until Hz is displayed, set the frequency to 10 KHz, and the Function to Sawtooth. Turn off Amplitude Modulation if it is turned ON.
- 11) Turn on channel A1 on the scope (All other 17 channels should be turned off.)
- 12) Set the Grid, Horizontal, Triggering, and channel A1 up as follows: Full, 50 us/division, autotrigger, DC coupling, triggering level about 2 V, 1 V/div, and GND symbol positioned 2 V below the grid centerline. The result should be a small, poorly-triggered sawtooth waveform.

CAUTION – USE OF AUTOSCALE: Although AUTOSCALE may be very useful for analog measurements, it often does not set things up well for accurate digital measurements. As a consequence, we usually do NOT use it. If you accidentally use AUTOSCALE and lose your settings, you can recover them by pressing Setup and Undo Autoscale.

- 13) Change the Display Select on the Wavetek to DC and adjust the value to 2.5 volts using the DC OFFSET; verify on the scope as you do this using Voltage Measure. Change the Display Select on the Wavetek to Vp-p and adjust the value to 5.00 V using the AMPLITUDE. Verify on the scope as you do this using Voltage Measure. You should now have a 10 KHz, 0.0 to 5.0 V sawtooth waveform on the scope. If you do not, make further adjustments or contact your instructor.
- 14) Turn off channel A1 on the scope and turn on channel A2.
- 15) Set up channel A2 at 1V/div with the GND symbol positioned 2 V below the grid centerline. You should see a waveform that looks like a pulse train.

VTC OBSERVATION

- 1) Turn on channel A1. You will now see two waveforms superimposed
- 2) Push **Main/Delayed** and set **Horizontal Mode** to **XY**. The transfer characteristic should appear. You will note that it has much sharper transitions than the example drawn in Figure 1-1. (In fact, the manufacturer has gone to great lengths to ensure this!) **Special Note:** High frequency noise feedback (from the rapidly changing output signal on the inverter back to the input signal) may badly distort the VTC. If it does, take two corrective measures before making measurements: 1) Remove the extension leads on the probes and carefully connect the grabbers directly to the pins, and 2) Successively select channels A1 and A2 and turn on BW Lim, the bandwidth limit.

1. Is the transfer characteristic that of an inverter? Explain.

FINDING NM_L AND NM_H

- 1) Press **Trace** on the scope, select **Mem1** and press **Save to Mem1**.
- 2) Carefully interchange the connection of the two probes to the black extension leads so that V_{IN} is on A2 and V_{OUT} on A1.
- 3) Press **Trace Mem1 on**. The original VTC and the mirrored VTC will now be displayed.
- 4) Press **Cursors** on the scope and **Clear all cursors**.
- 5) Select Y1 as the active cursor. Align Y1 with the lower right intersection of the VTCs to read out V_{OL} .
- 6) Select cursor Y2 and align with the upper left intersection of the VTCs to read out V_{OH} .
- 7) Select cursor X1 and attempt to align it with the leftmost -1 slope point to read out V_{IL} .
- 8) Select cursor X2 and align it with the rightmost -1 slope point on the same curve as in step 7 to read out V_{IH} .
- 9) Press **Stop** on the scope to get a more stable image.
- 10) Log in to a PC account at CAE (one team member) and, in the I volume, set up a folder for ECE351 and a folder for Exp1 within it.
- 11) Following the instructions on the course web page, use the **Word HP54600 Toolbar** to capture the scope image and save it to a file.
- 12) Save this image in the Exp1 folder of a team member.
- 13) In your report, add the following information to the image file printout.
 - a) a heading of 74HC04, the value of V_{CC} , and the team member names,
 - b) a label giving V_{OL} to one decimal place,
 - c) a label giving V_{OH} to one decimal place,
 - d) a label giving V_{IL} to one decimal place, and
 - e) a label giving V_{IH} to one decimal place.
- 14) **CHECKPOINT: Show the image on the computer screen to your instructor.**
- 15) Print enough copies of the image for all team members (Set printer name to **ece351**; backup printer is **ece554** through the door at the back of the lab).
- 16) Answer the following question:

2. Calculate and record NM_H and NM_L for the 74HC04. Compare these values to those calculated by referring to a 74HC04 datasheet (available on the course webpage). Try to explain any discrepancies.

74HC14 VOLTAGE TRANSFER CHARACTERISTIC AND NOISE MARGINS

Objective: To find the transfer characteristic and static noise margins for a 74HC14 HCMOS Schmitt-trigger inverter.

SETUP

- 1) The 74HC14 portion should be performed by the team member **not** performing the 74HC04 part.
- 2) Move the the probes from the 74HC04 to the 74HC14 by placing them on JP6-1 (channel A1) and JP6-2 (channel A2). The input signal connection from the Wavetek generator is already made using the same connection.

VTC OBSERVATION

- 1) The 74HC14 VTC should appear along with the stored 74HC04 VTC. If it does not, perform the necessary steps to obtain the two VTCs. Press Trace Mem 1 OFF to turn off the stored 74HC04 VTC. **Note:** It may be helpful to also observe V_{IN} and V_{OUT} using the normal scope time display to help make sense of the 74HC14 VTC.

FINDING NM_L , NM_H

- 1) Repeat the steps for finding NM_L and NM_H , this time for the 74HC14 including annotating, saving and printing the image.
- 2) Answer the following questions:

- 3a. Calculate and record NM_H and NM_L for the 74HC14.
- 3b. Discuss the differences in the transfer characteristics and switching levels of the two inverter types. How do they differ? Which inverter is superior based on your results, and why?

PROPAGATION DELAYS

Before measuring the propagation delays for HCMOS, we will examine the characteristics of the clock signal produced by the built-in oscillator.

MEASURING THE CLOCK CHARACTERISTICS

- 1) Turn off the Wavetek generator, then remove board power. Note that the Wavetek generator is no longer used after this point and can be disconnected.
- 2) Return the scope to its normal operating mode, and erase the contents of Mem1. Be sure to disable the Bandwidth Limits (BW Lim) on both channels, and remove the scope grabber connections to the board.
- 3) Using a black lead on the attached scope probe connect channel A1 to pin JP1-1 on the logic board.
- 4) Connect board power.
- 5) Adjust the scope appropriately to obtain a single cycle or so of the waveform. This is a clock signal generated on the logic board.

Use **Cursors** and **Measurement** to measure and record:

- 4a. the high and low non-peaking voltages
- 4b. the clock frequency, and
- 4c. the duty cycle (% of time the waveform is HIGH) of the clock.

6) CHECKPOINT: Have your instructor observe your clock waveform.

- 7) Print enough copies of the waveform for all team members.

SETUP FOR HCMOS DELAYS

The propagation delays for a single inverter will be measured by using three inverters connected as a chain. The first inverter in the chain provides a normal driving source and driving waveform shape and the last inverter in the chain provides a normal gate load for the second inverter on which the measurement is actually made. Between inverter outputs and inputs, permanent connections have already been made to JP1.

- 1) Remove board power.
- 2) Connect the scope probes from channels A1 and A2 to the JP1 pins 1 and 2, respectively, as shown in Figure 1-6 below.

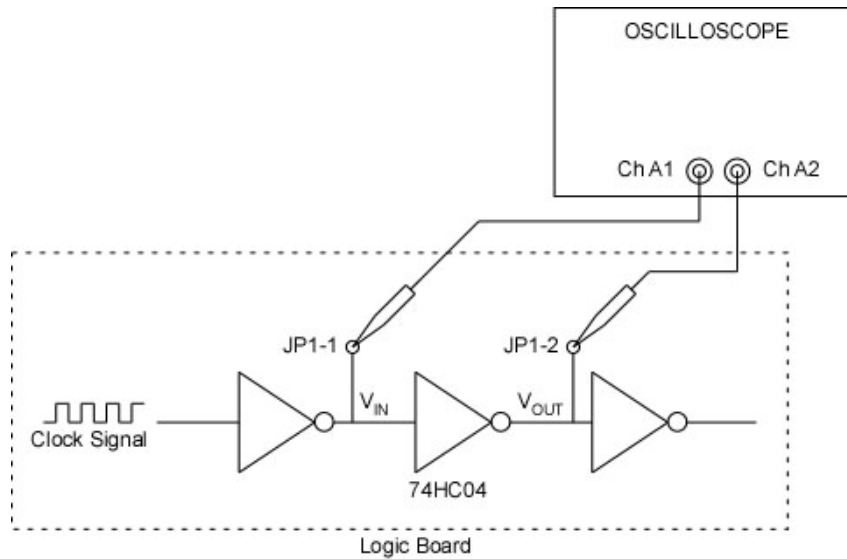


Figure 1-6 Setup for Finding Propagation Delay

MEASUREMENT OF CMOS DELAYS

- 1) Connect board power.
- 2) Be sure both scope channels are set to 1 V/DIV, accurately align the GND levels on the Ch A1 and Ch A2 waveforms and set TIME/DIV to 5 ns. At this point, the V_{IN} and V_{OUT} waveforms should appear and be aligned.
- 3) To measure t_{PHL} , set triggering to positive edge of A1.
- 4) Center the image so that a complete pair of V_{IN} and V_{OUT} waveform edges is visible.
- 5) Calculate $V_{50\%} = (V_{OH} - V_{OL})/2 + V_{OL}$ and align cursor V1 with this value.
- 6) Move cursor V2 so it does not appear.
- 7) Select cursor t1 and align with the intersection of V_{IN} and cursor V1.
- 8) Select cursor t2 and align with the intersection of V_{OUT} and cursor V1.
- 9) Read out the value for t_{PHL} .
- 10) Transfer, save, annotate and print the result for each team member. Annotate the axes and waveforms and include two labels: 1) part number and team member names, and 2) $t_{PHL} =$ (value) ns.
- 11) Change the triggering to negative edge and repeat all steps for t_{PLH} .
- 12) CHECKPOINT: Show your t_{PLH} measurement to your instructor.**
- 13) Answer the following.

5a. Use the measured t_{PHL} and t_{PLH} to find both t_{PD} and $t_{PD(average)}$.

5b. Compare t_{PD} and $t_{PD(average)}$ with the respective worst case(maximum) value, 19 ns, and typical value, 11 ns, as listed in the datasheet for the 74HC04 [3]. Explain the likely reason(s) for any differences.

LOGIC FUNCTION VERIFICATION

Objective: To determine the function of a logic gate using a counter to provide the inputs and the digital signal (logic analyzer) mode of the scope to observe the results. The logic gate you will examine has three inputs and a single output, and is purely combinational in nature (i.e. no sequential logic). The three inputs are connected to JP4 pins 1-3, and are driven by a counter built onto the logic board to provide the inputs for testing the gate. We will observe these inputs and the resulting logic gate output in order to determine the function of the logic gate

SETUP

- 1) Disconnect board power.
- 2) Remove the two scope probes and the connected black lead extensions.
- 3) Attach the ground for pod 0-7 of the logic analyzer to GROUND. Arrange the probe cables so that they are out of the way and the pod is at the back of the board.
- 4) Attach probes leads D0, D1, and D2 to the inputs, JP4-1, JP4-2, and JP4-3 respectively, and probe lead D3 to the output, JP4-4, as shown below in Figure 1-7.

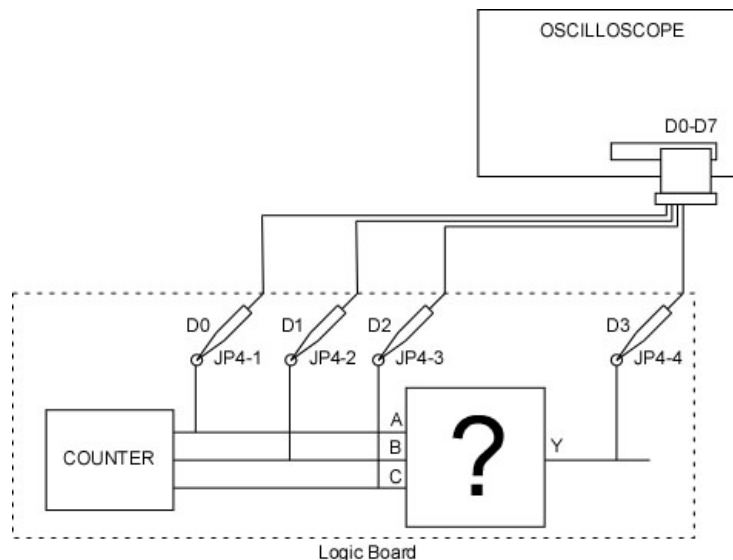


Figure 1-7 Setup for Determination of Logic Function

- 5) Return the scope to its normal operating mode, erase the contents of Mem1 and turn off channels A1 and A2.
- 6) Push D0 – D15 to activate the digital channels of the scope. Then turn ON channels D0 – D7.
- 7) Use the Entry or Select knob to select each of D4 through D7 and turn them off.
- 8) Push Labels/Threshold and select the Threshold Menu. Set the Threshold to TTL.
- 9) Press Previous Menu → Define Labels.
- 10) Turn Select to select bit_03.
- 11) Set the Position to the far left.
- 12) Use Entry to select characters and Copy to enter them to spell **Y**.
- 13) Press Assign Label to label bit_03 as **Y**.
- 14) Press Label -> ON.
- 15) Press Previous Menu and Display to return to display mode.
- 16) Press Main/Delayed and set the Time Ref to Left.
- 17) Connect board power.

- 18) Set the Time/Div to 5 μ s. Set up negative edge triggering on signal D2. Why D2? Because it has only one negative edge per repetitive cycle of the counter output. If you do not get a stable display, advance the Holdoff to a bit over 4 μ s. Is the display now stable (if perhaps a bit "jittery")? The reason the display may not have been stable is that there were "glitches" in D2 which produced additional negative edges notably halfway between the expected negative edges. Holdoff prevents the scope from triggering again until after the value set and thus avoids triggering on the glitch edge. Holdoff is also useful for triggering on more complex periodic signals not containing glitches as well.
- 19) For a logic analyzer type instrument, pattern-triggering is an alternative which is somewhat less likely to have a triggering problem than edge-triggering. Press Pattern.
- 20) Using Entry to select the signals, set up the following triggering pattern: D0=L, D1=L, D2=L. Change Holdoff to see if it is necessary to achieve stable triggering.
- 21) Position the waveform so that (D0, D1, D2) = (0, 0, 0) is in the second position from the left on the grid, i. e., just to the right of the labels, and the entire waveform through (D0, D1, D2) = (1, 1, 1) appears.
- 22) Adjust the scope time base so that 1/2 period of the highest frequency waveform occupies one grid division Use the scope Vernier to do this. The Vernier can be turned on using the Main/Delayed menu. With the Vernier on, the Time/Div adjustment is much finer.

OBSERVATION

- 1) Answer the following.

6. What is the logical function of this gate [$Y = f(A,B,C)$]? Explain how you determined this from the displayed waveforms.

- 2) **CHECKPOINT: Show your logical function result to your instructor.**
- 3) Save the scope image in the Exp1 folder and print a copy for each team member.

REPORT

Your individual report on 8.5 by 11 inch pages should follow the report format available on the course web page and consist of:

- 1) A cover with the experiment number, experiment name, your name, name(s) of other team member(s), and your instructor's name,
- 2) Description of Laboratory Exercise and Conclusions as shown in the report format,
- 3) Your individual answers to all of the questions given in the green-bordered boxes (online version has color), and
- 4) Copies of all printouts for the lab properly annotated and in the order produced.

CONCLUSION

This completes the lab. The information learned here will be very valuable in performing the remaining experiments. Note that this lab experiment is a guide to using the oscilloscope and some aspects of the prototyping boards. Please keep it and refer back to it during other experiments; do not turn it in with your report! Don't guess! You may get incorrect results or, worse, burn out something!

REFERENCES

1. MANO, M. M AND C. R. KIME. *Logic and Computer Design Fundamentals*, 1st and 2nd ed. Upper Saddle River, NJ: Prentice Hall, 1997 and 2000.
2. KANG, S-M. AND Y. LEBLEBICI. *CMOS Digital Integrated Circuits - Analysis and Design*, 2nd ed. Boston: McGraw-Hill, 1999.