

Department of Electrical and Computer Engineering  
University of Wisconsin-Madison

**ECE 453**  
**EMBEDDED MICROPROCESSOR**  
**SYSTEM DESIGN**

Course Syllabus

Spring 2009

Michael G. Morrow  
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ACKNOWLEDGEMENTS

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**Plexus Technology Group**  
**Texas Instruments**  
**Intel Corporation**  
**Microsoft**  
**PCMCIA**

COURSE INFORMATION

PREREQUISITES/OTHER COURSES:

ECE 315, ECE 353

Our past experience has shown that students who have not yet completed these courses (or equivalents) end up earning lower grades in this course. Failure to complete the prerequisites will not be accepted as an excuse for poor performance. Exceptions may be granted for ECE 315 for students with other microprocessor experience or for concurrent registration in ECE 315.

ECE 453, 468, and 554 are each intensive 4-credit courses that demand a great deal of your time outside of scheduled class hours. It is unwise to attempt to take more than one of these courses at a time. Please be aware that you are expected to complete your assignments on time even if you have a busy workload in other courses.

LECTURE AND EXAMS

As you can see from the course topics list on the course schedule, the lectures will vary among discussions of various interfacing, software development, and embedded systems design topics. Please note that these topics are tentative and subject to some change based on instructor and/or student interests. There will be one final examination. The questions will be based on the objectives of the topics presented in lecture, with a mixture of analysis and design problems. In addition, the final examination may contain specific questions directed at each expert team's area of expertise.

ATTENDANCE:

Regular attendance is expected for both the lectures and scheduled lab exercises. You are responsible for everything discussed in lecture, and collecting any handouts that you miss. Assignments must be turned in at the prescribed time. Changes to assignment deadlines will only be considered under the most exceptional circumstances.

Project teams may have persons from more than one lab section. Students may attend either lab section to work as a team.

PROJECT HARDWARE:

Each project team will be furnished with a development board containing a Xilinx Spartan FPGA and a Freescale i.MX21 microprocessor based on an ARM926 core, a prototyping card, and numerous accessories. These materials have a value in excess of \$1,500.00, so it is expected that they will be treated with the utmost care and returned in working condition at the end of the semester. For project teams that wish to keep their project hardware, it may be possible to keep the prototyping card, but not the development board. All additional parts for projects will be purchased at student expense.

The development boards are not to be removed from 3605EH except for storage in the project lockers outside. All transfer and handling of hardware will be done in an ESD-safe manner.

COURSE CONDUCT

TIMETABLE

Lecture: 1:20-2:10pm MWF  
Location: 3534 Engineering Hall  
Labs: 3605 Engineering Hall  
Lab 301: Monday 2:25-5:25pm  
Lab 302: Tuesday 2:25-5:25pm

INSTRUCTOR

Name: Michael G. Morrow  
Office: 3537 Engineering Hall, 265-9007, [morrow@engr.wisc.edu](mailto:morrow@engr.wisc.edu)  
  
Office hours: Posted on the web at  
<http://eceserv0.ece.wisc.edu/~morrow/schedule.htm>

TEACHING ASSISTANT

Name: Dan Seemuth  
Office: TBA  
Office Hours: TBA

STUDENT RESPONSIBILITY

This course focuses on the design of microprocessor-based systems using off-the-shelf components. The intent of this course is that each project team will create an independent design. In this course, it is expected that you will define a project idea, design the hardware and software, determine a suitable test plan, then build and verify the actual device's operation while working in a 3-person team. There are a number of graded assignments during the course of the semester; however, a working project at the end of the semester is an essential measure of success.

You are responsible for all assigned reading material and all lecture content unless otherwise specified by the instructor. If you miss class or lab, it is your responsibility to obtain assignments and other information given on the days you missed.

All work that you submit in this course is expected to be own, or the product of your team for team assignments and project deliverables. If you use work attributable to others (i.e. application notes, examples, etc.), ensure that proper credit is given to the original author. Evidence indicating inappropriate copying of work from others or other prohibited cooperation will be dealt with as academic misconduct. Acceptable types of assistance you may offer to or receive from others are limited to assisting in problem interpretation, and occasional general hints on ways of attacking a problem. If in doubt, see the instructor or teaching assistant.

### GRADING

Grading will be based on the following breakdown;

Individual and expert team assignments	10%
Final Examination	15%
Quality and Effort	10%
Design Project	65%
Deliverable #1	3%
Initial project proposal	
Deliverable #2	5%
Detailed proposal, work schedule, cost/time estimate	
Deliverable #3	5%
Requirements definition, updated schedule and cost/time estimate	
Deliverable #4	12%
Basic register file design/implementation	
Timing analysis	
Deliverable #5	10%
Schematic diagram, FPGA block diagram, test plan, updated schedule and cost/time estimate	
Design review	
Deliverable #6	10%
Initial hardware test	
Deliverable #7	15%
Final demonstration of project	
Deliverable #8	5%
Final project report	
	100%

All members of a team will receive the same grade for project deliverables and team assignments. The quality and effort grade will be assigned by your instructors to reflect your

participation in class activities, your attitude and professionalism, your contributions as a project team member, and your effectiveness as an expert team member.

#### EXPERT TEAMS

Each student will be assigned to one expert team in addition to their design team. It is expected that all students will work to become experts in their assigned area, and assist project teams with problems in that area. Only one student from each project team can be a member of any given expert team. Expert teams may be required to give a presentation or conduct a class in their area of expertise. Expert team specializations will be determined early in the semester.

#### PROJECT SPONSORSHIP

Plexus Technology Group has offered to sponsor an indeterminate number of student projects. This sponsorship opportunity is solely between the student team and Plexus Technology Group. Students should apply directly to Plexus Technology Group for sponsorship of their projects, according to the criteria published by Plexus Technology Group. Detailed information will be distributed in class.

#### FIELD TRIP

A class field trip is planned to visit Plexus Technology Group in Neenah, Wisconsin. The exact timing of this trip will be discussed and finalized in class. All students are expected to attend. Transportation will be provided. Plexus has agreed to offer an overview of the design process, several expert guest lecturers, and a tour of the engineering and manufacturing areas.

#### PROJECT AWARDS

At the final project demonstration, one project may be selected as 'best in class'. The team members receiving this distinction, and who have satisfactorily completed all prior course requirements, will receive an overall **A** grade in the class. The determination of 'best in class' is solely at the discretion of the instructor, and will be based on an overall evaluation of the project's ingenuity and complexity, the team's performance on deliverables, and the features and functionality of the finished project.

### DELIVERABLES REQUIREMENTS

The specific requirements for the course deliverables are as outlined below. Unless otherwise specified, all submitted deliverables are due by 5:00pm Friday of the week indicated in the course schedule. Performance deliverables (i.e. demonstrations) are to be completed in the scheduled lab periods of that week. No credit will be given for late deliverables without prior approval of the instructor.

In addition to the below requirements, all submitted deliverables will have a title page indicating the team number, team members, the title of their project, and the deliverable type. Documents should be written as technical documents, in the third person, and should be professional in appearance (i.e. no hand drawn diagrams, etc.).

In addition to the specified deliverables, starting in week 6 **each design team will submit by 5pm Friday a weekly status report** by email to the instructor and lab TA. This shall be a 2-3 paragraph narrative describing the team's progress to date in both a qualitative and quantitative manner. Specifically, it must include the following;

- a. Whether the project is ahead, behind, or on schedule.
- b. An assessment of % completed versus % planned versus % of semester-gone-by. Address those activities that are ahead or behind schedule.
- c. If significant schedule slippage has occurred, include a plan describing how the team will recover.
- d. A general description of the team's progress, major issues, and expected progress in the next week.

#### **#1 - Initial project proposal**

The initial project proposal shall be a brief summary of the team's project idea. A one-page formal memorandum will provide a short summary of the design problem and a brief description of the project's operation and features. A functional block diagram of the proposed device shall be included on a separate page.

**#2 - Detailed proposal, work schedule, cost/time estimate**

The detailed proposal will consist of an executive summary, a description of the problem to be solved, a functional block diagram and a narrative explanation of describing how your project will be organized/how it will work, and description of the project features. Prepare and submit a cost estimate and a Gantt chart detailing the scheduled activities, the individual(s) responsible, and the expected work time (in hours) for each activity. The Gantt chart should be in sufficient detail to be useful as a tool to monitor progress. The activity breakdown should mirror the functional breakdown of the project, and shown the sequential dependencies in the project work. The course deliverables should be shown on the schedule. The schedule will be prepared and maintained using Microsoft Project software, which is available on the lab computers and at some CAE labs.

Each team will also present their project proposal to the entire class. Each team will be allotted approximately 5 minutes to make their presentation. It is expected that all presentations will be made using presentation software, and present a professional image of the project team.

**#3 - Requirements definition, updated schedule and cost/time estimate**

The requirements definition will explicitly define the detailed functional capabilities of your device, i.e. under what conditions it must operate, how it will respond to inputs, output characteristics, etc. The requirements definition will be the basis for the test plan that you develop later, so it should be written with that in mind.

An updated schedule and cost/time estimate (including one paragraph narrative analysis) will also be submitted indicating actual progress and any adjustments to the projected cost or work effort. Sample requirements definition formats will be distributed in class.

**#4 - Basic register file design/implementation and timing analysis**

Using the FPGA, create a register file consisting of eight read-access registers and eight write-access registers. All registers are to be 32-bits wide, and are to be mapped to addresses in the i.MX21 /CS5 memory space (0xD3000000-0xD3FFFFFF). The register file shall be a synchronous design based on the 100MHz FPGA clock. The read-access registers will return the data last written to the write-access register at the same address, except the read-access register at the lowest address will instead return the number of write operations to the register file in the upper half-word and the number of read operations in the lower half word, as shown below;

	read-access register data	
address	31	16 15 0
0xD3000000	number of writes to registers	number of reads from registers
0xD3000004	write-access register data[31:0]	
0xD3000008	write-access register data[31:0]	
...	...	

The register at 0xD3000000 must be accessible as a word only (ignore byte/half-word transfers), while the other registers must support byte, half-word, or word accesses. Writes to

0xD3000000 should have no effect. Do not count reads or writes to 0xD3000000.

Create a Linux application to easily access the four registers to test for proper operation. Also, the application will have the ability to perform a series of 65,535 transfers to and from address 0xD3000004 to verify correct operation. The data for each transfer shall consist of the 32 values that have just a single 1 bit, followed by 65,503 words of random data. Report the total number of transfers and the number of errors when the test completes. (After every write to address 0xD3000004, you must do a write of a different value to a different address in the /CS5 region. Try a test with an unconfigured FPGA to see what happens if you don't.)

The registers may be decoded as exhaustively (or as non-exhaustively) as you desire, so long as the required functionality is obtained. Be sure to synchronize signals appropriately. The register set deliverable will be demonstrated in lab.

Complete an analysis of the timing margins for memory reads/writes to the registers you created. Note that this is an analysis, so it is NOT based on *measurements* of the timing; rather you are determining whether the timing works based on the specifications of the parts involved. (Of course, it would seem a bit foolish not to do a few measurements to verify your calculations.)

The specific requirements for the timing analysis deliverable are that you will determine the timing margins for both a read and a write to the register at address 0xD3000004. Be sure to clearly identify all sources of delays, and provide a simplified block diagram showing the relevant signal paths and delays. Draw a waveform diagram showing how the timing equations are derived, write the symbolic equations, and then solve them using the appropriate values.

Additional information will be provided regarding the memory interface timing and signal paths within the development platform. Your results will be evaluated on the basis of both technical correctness and on how clearly you present the information.

Submit a paper copy of the Verilog code for your register file with the timing analysis, along with answers to the following;

1. What happened when you ran the register test with an unconfigured FPGA and only doing write-read from 0xD3000004? Why?
2. Explain how you read/write counting logic works.

**# 5 - Schematic diagram, FPGA block diagram, test plan, bill of materials (BOM), updated schedule and cost/time estimate, Design Review**

The schematic diagram shall show all circuitry in your project, and shall be drawn using one of the available CAD packages. The prototyping board and evaluation boards do not need to be shown at the component level, but should be shown at the block level where they interconnect to your circuitry. All connections to any other external devices will be shown. The schematic diagram must show all pins of all devices, and all connections to the prototyping board. All integrated circuits shall be clearly identified by part number. All passive components shall have values indicated. All components shall be enumerated using standard designators (R1, R2, etc.). **The schematic diagram should be in sufficient detail that your circuit can be built by referring only to the schematic diagram and BOM.**

Provide a block diagram in sufficient detail to show the design of your FPGA logic. At a minimum, it should include the major functional units and their ports, and the interconnecting signals.

The test plan will enumerate in detail how you will be able to demonstrate conclusively (and over what range of parameters) that your project is indeed functional. The test plan should naturally follow from your requirements definition.

The BOM will list all parts required for your design, including manufacturer/supplier, part number, quantity, and unit cost, and show an aggregate cost for the project. The BOM should be kept in a spreadsheet to allow easy changes.

An updated schedule and cost/time estimate will also be submitted indicating actual progress and any adjustments to the projected cost or work effort.

Each team is also required to present their design to the instructors as a formal design review (not a marketing presentation) in the lab. In this review, you will be expected to discuss your overall design organization, your FPGA logic organization, the external interfaces to/from the FPGA, external devices and signals, how you chose additional parts that are added to the platform, and any other relevant items. It is expected that the review will present a professional image of the project team. Be prepared to justify your design decisions.

**#6 - Initial hardware test**

Demonstrate your hardware's functionality based on your test plan requirements. Final software does not have to be available at this time, only your test software. You may use multiple software applications and/or FPGA configurations to demonstrate different portions of the hardware if you have not finished integrating the hardware/software support for all hardware functions.

**#7 - Final demonstration of project**

Execute your test plan to demonstrate your hardware and software functionality. There is no report due for this deliverable. Grading will be based on your instructor's assessment of your project's functionality, complexity, and efficiency of design, your demonstrated understanding of its operation, and your ability to present your project in a professional manner.

**#8 - Final project report**

The final report will be comprised of an executive summary of the project, a general discussion of how well your project met your requirements, and detailed evaluations of how well your project performed according to your test plan, how accurate your schedule/cost/time estimates were (include a final cost/time report indicating actual effort and cost expended) and your assessment of how effective your test plan was in determining your project's functionality. Attach an appendix indicating "lessons learned" during the course of the semester. An as-built paper schematic of all external circuitry, a block diagram of the FPGA logic, and a CD containing the complete project directories of all relevant software will also be submitted.

TENTATIVE COURSE OUTLINE

Week #	Start	# of Lec	Topic(s)	Events
1	Jan 19	2	Course Introduction Design Process and Milestones	Team formation. No labs.
2	Jan 26	3	i.MX21 architecture	<a href="#">Lab – Introduction/Soldering</a>
3	Feb 2	3	Development platform Development tools	#1 Initial project proposal due (in lab) <a href="#">Lab – FPGA Intro</a>
4	Feb 9	3	Embedded operating systems Embedded applications and device drivers	<a href="#">Lab – Linux Intro</a>
5	Feb 16	3	Component selection Power supplies <a href="#">Project Presentations</a>	#2 Detailed proposal, work schedule, cost/time estimate due. <a href="#">Lab – Linux Applications</a>
6	Feb 23	3	Interfacing sensors Interfacing audio and speech	<a href="#">Lab – Linux/FPGA</a> *** <a href="#">Plexus plant tour?</a> ***
7	Mar 2	3	Buses and memory Low-power design	#3 Requirements definition, updated schedule, and updated cost/time estimate due.
8	Mar 9	3	Motors and heatsinking	#4 Register set and timing analysis deliverable due in lab.
9	Mar 16	3	<a href="#">Spring Break!</a>	
10	Mar 23	3	Advanced buses (PCI, USB)	#5 Schematic diagram, test plan, BOM, updated schedule, and updated cost/time estimate due.
10	Mar 30	3	Progress meetings	#5 Design reviews in lab.
11	Apr 6	3	Final exam	
12	Apr 13	3	Progress meetings	<a href="#">Engineering Expo</a>
13	Apr 20	3	Progress meetings	#6 Initial hardware test.
14	Apr 27	3	Progress meetings	
15	May 4	3	Course wrap-up	#7 Final project demonstrations. #8 Final project report due. *** <a href="#">Project open house on Friday</a> ***

## LAB RULES

1. Food, drink, and smoking are not permitted in the lab.
2. Working with others. The design project will be completed in small groups. Groups with more than three members or with members in multiple lab sections require approval of the course instructor. The free interchange of ideas, concepts, and specifics within a group is necessary and encouraged. However, the use of designs and software from previous class projects is expressly prohibited, as is the use of work from students outside the group with the exception of advice received from a designated student 'expert' in their area of expertise.
3. Use of another person's work. You may use ideas from datasheets, application notes, and the like, without permission. You must obtain permission from the course instructor to use any other work produced by another person, including work from current or previous projects, with exception of advice received from an expert team. In all cases, you are required to attribute the work to the original source.
4. Handling of another person's property. Do not touch another person's work without their permission – this includes 'playing' with a project, moving a project so you can work, or deleting someone else's files. Damage caused to another student's project is defined by the UW System as Academic Misconduct. Disciplinary action may include expulsion; it does not matter if the intent was malicious. However, if a project's owner gives another student permission to handle his/her project, any damage that occurs is the responsibility of the project owner.
5. Computer software. No software is to be copied from a lab computer. No software is to be transferred between or removed from the lab computers.
6. Lab equipment. Abuses of lab equipment will not be tolerated. Do not remove or change scope probes or logic analyzer pods. When probing circuits, use an additional wire instead of removing the probe clips or tips. Turn off power supplies, monitors, scopes and analyzers when not using them. No equipment is to be removed from the lab room!
7. Broken equipment. Please attach a note to any equipment that seems to be broken indicating the current date and the nature of the problem. Inform your TA as soon as possible so that the equipment can be tested and repaired.
8. Soldering. You may only solder at the designated bench in the lab. Please turn off the soldering irons when you are finished. You will receive an introduction to soldering practice at the start of the course. Please feel free to see the instructor for additional instruction and/or help if you need to solder very small or difficult parts.
9. High-voltage. If your project plugs directly into an AC outlet (e.g. you add your own power supply), or if it uses AC voltages greater than  $30V_{RMS}$  or DC voltages greater than 45V, then you must follow special precautions for high-voltage use. Your TA must

approve of your design and inspect your work before you will be allowed to plug it into a receptacle. Use the ground-fault circuit interrupter (GFCI) receptacle for your project, and the regular receptacles for lab equipment. All conductive surfaces must be insulated, preferably with heat-shrink tubing. If you use a metal chassis or enclosure, it must be grounded. All accidents must be reported to an instructor.

10. Telephones. Phone lines in the lab room have been installed for use in projects. Their use is restricted to campus calls only.
11. Printers. The laser printers used in the lab room are for ECE 315, 453, and 468 only. Any printouts unrelated to these courses will be confiscated and destroyed.
12. Lab upkeep. Please clean up all miscellaneous wires, parts scratch paper, newspapers, and trash before you leave.
13. Security. You will be provided with 24-hour access to the lab room. You may not share this code with others. Please do not prop open doors.
14. Monitoring of the lab. The lab room is monitored at all times by several video cameras. Should difficulties occur, recordings of the room may be used to identify and discipline the person(s) who is (are) responsible.